ARM1156T2(F)-S Hardware Design

Summary:
This course is designed for those who are designing hardware based around the ARM1156T2(F)-S core. Including an introduction to the ARM product range and supporting IP, the course covers the ARM core range and AMBA on-chip bus architecture. The ARM debug architecture, real-time trace solution and simulation models are also covered. The course includes a number of worked examples to reinforce the lecture material.

Prerequisites:
- Some knowledge of embedded systems.
- Familiarity with digital logic or hardware / ASIC design issues.
- A basic awareness of ARM is useful but not essential.

Audience:
Hardware design engineers who need to understand the issues involved when designing SoC's around the ARM1156T2(F)-S core.

Length:
4 days

Modules:
- The ARM Architecture
- ARM CPU Architectures
- Memory Sub-systems
- Memory Management
- Memory Access Behavior
- ARM1156 Overview
- ARM1156 Instruction Sets
- Exception Handling
- AHB Protocol
- AXI Protocol
- AXI Interconnection Architectures
- NIC-301 Network Interconnect
- APB
- Primecell VIC
- ARM1156 Processor Core
- ARM1156 L1 Sub-Systems
- ARM1156 L2 Interfaces
- ARM1156 Implementation
- ARM1156 Example System
- ARM1156 Clocks, Resets & Power Management
- ARM1156 Memory Protection
- ARM1156 Booting
- ARM1136/76 Interrupts
- ARM1156 Multi-processor synchronization
- ARM1156 L2 Caches
- ARM11 Coprocessors
- ARM11 Invasive Debug
- ARM11 Non-Invasive Debug
- ARM Processor Simulation Models
- ARM1156 Integration