



ARM926EJ-S Hardware Design

Summary:

This course is designed for those who are designing hardware based around the ARM926EJ-S processor core. Including an introduction to the ARM product range and supporting IP, the course covers the ARM core range and AMBA on-chip bus architecture. The ARM debug architecture, real-time trace solution and simulation models are also covered. The course includes a number of worked examples to reinforce the lecture material.

Prerequisites:

- Some knowledge of embedded systems
- Familiarity with digital logic and hardware/ASIC design issues
- A basic awareness of ARM is useful but not essential

Audience:

Hardware design engineers who need to understand the issues involved when designing SoC's using the ARM926EJ-S processor core.

Length:

4 days

Modules:

- The ARM Architecture
- ARM CPU Architectures
- Memory Sub-systems
- Memory Management
- Memory Access Behavior
- ARM v4T
- ARM v5TE(J)
- Thumb
- Exception Handling
- AHB Protocol
- AHB Connection Architectures
- APB
- AMBA Design Kit
- Primecell VIC
- ARM926EJ-S Processor Core
- ARM926EJ-S System Interfaces
- ARM926EJ-S Implementation
- ARM926EJ-S Memory Management
- ARM926EJ-S Coprocessor I/f
- Initializing ARM Processors
- Debugging an ARM-based System
- Tracing an ARM-based System
- ARM Processor Simulation Models
- ARM926EJ-S Integration