

ARM Cortex-A53 MPCore Hardware Design

Summary:

This course is designed for those who are designing hardware based around the Cortex-A53 MPCore processors.

Prerequisites:

- Comprehensive knowledge of the ARMv8-A architecture (see notes below)
- Familiarity with the AMBA on-chip bus architecture
- Knowledge of embedded systems
- Experience with digital logic and hardware/ASIC design issues

Audience:

Hardware design engineers who need to understand the issues involved when designing SoCs around the ARM Cortex-A53 MPCore processor.

Course Length: 3 days

Modules:

- Cortex-A72/A53 Processor Overview
- ARMv8 Architecture Overview
- Cortex-A53 Processor Core
- Cortex-A72/A53 Memory Management Unit
- Cortex-A53 Memory Sub-Systems
- Cortex-A72/A53 Clocks and Resets
- Cortex-A72/A53 Power Management
- CCI-400 Cache Coherent Interconnect (or CCN-504 Cache Coherent Network)
- GIC-400 Interrupt Controller (or GIC-500 Interrupt Controller)
- Cortex-A72/Cortex-A53 System Design Considerations
- Cortex-A72/A53 Debug
- Cortex-A72/A53 Booting
- Cortex-A53 Configuration
- Cortex-A72/A53 Integration Summary

Notes:

For students who do not have the pre-requisite knowledge of the ARMv8-A architecture and AMBA, we provide an optional one-day introductory course on these subjects.