ARM Cortex-A5 Hardware Design

Summary:
This course is designed for those who are designing hardware based around the Cortex-A5 uni-processor.

Prerequisites:

- Some knowledge of embedded systems
- Familiarity with digital logic and hardware/ASIC design issues
- A basic awareness of ARM is useful but not essential

Audience:
Hardware design engineers who need to understand the issues involved when designing SoC's around the ARM Cortex-A5.

Length:
3+ days

Modules:

- Introduction to the ARM Architecture
- Cortex-A5 Overview
- Cortex-A5 Processor Core
- TrustZone Overview
- Cortex-A5 Memory Management
- Cortex-A5 UP Memory Sub-Systems
- Cortex-A5 UP Clocks, Resets & Power Management
- Introduction to AMBA3
- NIC301 AMBA Interconnect
- L2C-310 Level-2 Cache Controller
- Cortex-A5 Interrupt Controller
- Introduction to CoreSight
- Cortex-A5 Debug
- Cortex-A5 Booting
- Cortex-A5 UP Configuration & Deployment
- Cortex-A5 Reference Methodology
- Cortex-A5 Integration

Notes:
For students who do not have the pre-requisite knowledge of the ARMv7-A architecture and AMBA, we provide an optional one-day introductory course on these subjects.