ARM Cortex-A9 MPCore Optimized Macrocells (Osprey) Hardware Design

Summary:
This course is designed for those who are designing hardware based around the Cortex-A9 MPCore multiprocessor.

Prerequisites:
- Some knowledge of embedded systems
- Familiarity with digital logic and hardware/ASIC design issues
- A basic awareness of ARM is useful but not essential

Audience:
Hardware design engineers who need to understand the issues involved when designing SoC's around the ARM Cortex-A9 MPCore multiprocessor.

Length:
4 days

Modules:
The ARM Architecture
Cortex-A9 Instruction Sets
ARM v6 Memory Types
Memory Management
ARMv6 VMSA
Exception Handling
Introduction to TrustZone
CPU Architectures
Memory Sub-systems
Introduction to SMP & MESI
(Optional IEM)
AXI Protocol
AXI Interconnection Architectures
NIC301
AMBA Designer
APB
Cortex-A9 MPCore Optimized Macrocells Overview
Cortex-A9 Processor Core
Cortex-A9 L1 Sub-Systems
Cortex-A9 MPCore Sub-systems
Cortex-A9 MPCore Interrupt Controller
Cortex-A9 MPCore L2 Interfaces
Cortex-A9 Memory Management
Initializing Cortex-A9 MPCore based Systems
L2CC – PL310
Introduction to CoreSight
Cortex-A9 Invasive Debug
Cortex-A9 Non-Invasive Debug
C-A9 MPCore Optimized Macocells functional Integration
C-A9 MPCore Optimized Macrocells Clocks, Resets & Power Management
C-A9MPCore Optimized Macrocells Physical Integration