ARM Cortex-R4 Hardware Design

Summary:
This course is designed for hardware engineers designing systems based around the ARM Cortex-R4 processor core. Including an introduction to the ARM product range and supporting IP, the course covers the ARM core range, programmer's model, instruction set architecture and AMBA on-chip bus architecture. The Cortex-R4 debug architecture is also covered. The course includes a number of worked examples to reinforce the lecture material.

Prerequisites:

- Some knowledge of embedded systems
- Familiarity with digital logic and hardware/ASIC design issues
- A basic awareness of ARM is useful but not essential

Audience:
Hardware design engineers who need to understand the issues involved when designing SoC's around the ARM Cortex-R4 processor core.

Length:
4 days

Modules:

- Architecture ARMv7-A/R Overview
- ARMv7-A/R Applications Level Programmer’s Model
- ARMv7-A/R System Level Programmer
- ARMv7-A/R Memory Model
- ARMv7-R Protected Memory System Architecture
- ARMv7-A/R Exceptions
- Micro-Architecture: Pipelines
- Micro-Architecture: Memory
- AXI-Protocol
- Cortex-R4 Overview
- Cortex-R4 Processor Core
- Cortex-R4 L1 Sub-Systems
- Cortex-R4 L2 Interfaces
- Cortex-R4 Error Handling Schemes
- Cortex-R4 Clocks, Resets & Power Management
- Cortex-R4 Implementation
- Cortex-R4 Initialization
- Cortex-R4 Interrupts
- Cortex-R4 and Vectored Interrupt Controller – PL192 (Optional)
- Introduction to CoreSight
- Cortex-R4 Invasive Debug
- Cortex-R4 Non-invasive Debug
- Cortex-R4 Integration
- Level 2 Cache Controller – L2C-310
- Generic Interrupt Controller – PL390
- AHB Protocol
- AXI Interconnection Architectures
- NIC-301