ARM Cortex-R7 MPCore Hardware Design

Summary:
This course is for engineers who will integrate the Cortex-R7MPcore in to an SoC design. It assumes no knowledge of ARM processors or associated bus protocols. It starts by introducing the essential ideas of the ARM architecture, micro-architecure and bus protocols. It then looks at the main blocks and behaviours of the C-R7MPcore. It also introduces CoreSight debug infrastructure and the embedded debug features of the C-R7 processors.

Prerequisites:

- Some knowledge of embedded systems
- Familiarity with digital logic and hardware/ASIC design issues
- A basic awareness of ARM is useful but not essential

Audience:
Hardware design engineers who need to understand the issues involved when designing SoC's around the ARM Cortex-R7 processor core.

Length:
4 days

Modules:

- Architecture ARMv7-A/R Overview
- ARMv7-A/R Applications Level Programmer’s Model
- ARMv7-A/R Memory Model
- ARMv7-R Protected Memory System Architecture
- ARMv7-A/R Exceptions
- Micro-Architecture: Pipelines
- Micro-Architecture: Memory
- Introduction to SMP & MESI
- AXI Protocol
- Cortex-R7 MPCore Overview
- Cortex-R7 Processor Core
- Cortex-R7 L1 Sub-Systems
- Cortex-R7 MPCore Sub-Systems
- Cortex-R7 MPCore L2 Interfaces
- Cortex-R7 Fault Tolerance Support
- Cortex-R7 MPCore Clocks, Resets & Power Management
- Cortex-R7 Interrupt Controller
- Cortex-R7 Initialisation
- Cortex-R7 MPCore Configuration
- Cortex-R7 MPCore Implementation
- Introduction to CoreSight
- Cortex-R7 Invasive Debug
- Cortex-R7 Non-invasive Debug
- Cortex-R7 Integration
- Level 2 Cache Controller – L2C-310
- AXI Interconnection Architectures
- NIC-301