Designing with CoreSight

Summary:
This course is intended for engineers designing silicon devices based around ARM cores incorporating the CoreSight debug architecture. The course covers an introduction to CoreSight and then presents detailed material on each aspect of the technology. Please note that the course assumes familiarity with ARM-based designs and with the AMBA/AXI on-chip bus architecture.

Prerequisites:

- A working knowledge of system-on-chip design.
- Familiarity with ARM technology.
- Familiarity with AMBA/AXI.

Audience:
Hardware design engineers who need to understand and work with the CoreSight debug architecture.

Length:
2 days

Modules:

- CoreSight Overview
- CoreSight Buses
- Programmer's Model
- ETM Specification
- System Discovery
- Control & Access (Debug Access Port, APB Interconnect, Embedded Cross Trigger)
- Trace Sources (CPU Trace Macrocells, System Trace Macrocell, Instrumentation Trace Macrocell)
- Trace Links (Trace Funnel, Replicator, ATB Bridge)
- Trace Sinks (Trace Port Interface Unit, Embedded Trace Buffer, Trace Memory
- Controller)
- Clocks, Reset & Power Management
- System Design
- Using CoreSight SoC